REMARKS

Reconsideration of the application is requested.

Applicant acknowledges the Examiner's confirmation of receipt of applicant's certified copy of the priority document for the German Patent Application 199 54 346.1, filed November 11, 1999 supporting the claim for priority under 35 U.S.C. § 119.

Claims 1-27 are in the application. Claim 1 has been amended.

In "Claim Rejections - 35 USC § 112 SECOND PARAGRAPH" item 3.0 on page 1 of the Office Action mailed January 14, 2004 (just prior to the above-identified Office Action) claims 1-27 were rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, in item 3.1 the Examiner stated:

> it is unclear to the Examiner how the memory device is operatively connected, e.g., how the memory cells, the comparison units and address applied to the memory device are linked to perform intended functionality.

Although the Examiner's assumption that the "address is applied to the comparator units" was partially correct, Claim 1 has been amended in an effort to clarify how the address

input is configured to receive "**at least a portion of an address**" applied to the memory device.

Support for these changes may be found on pages 2-3 and 16-19 of the specification of the instant application. Additional support may be found in FIG. 1 and FIG. 5, which are described on pages 1-4 and 11-20 of the specification of the instant application.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In "Claim Rejections - 35 USC § 103" item 3.2 on page 1 of the above-identified final Office Action, claims 1-27 have been rejected as being obvious over U.S. Patent No. 6,202,180 to *Nose* (hereinafter **NOSE**) in view of U.S. Patent No. 4,639,915 to *Bosse* (hereinafter **BOSSE**) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a memory device including:

> a multiplicity of memory cells for storing data;
>
> comparison units connected to the memory cells and each having an address input for receiving **at least a portion of an address** applied to the memory device, the comparison units being configured **to simultaneously check** whether the address applied to the memory device is associated with at least one memory cell which cannot be properly written to or read out or **to simultaneously check** whether the address applied to the memory device is located in a memory cell area containing memory cells which cannot be properly written to or read out; and
>
> in a testing phase of the memory device, the comparison units being placed into a testing state different from a state during a normal operation of the memory device.

Thus, as previously indicated, the comparison units of the instant application are individually assigned to specific memory cells or memory cell areas. The comparison units operate in parallel so that the **at least a portion of an address** applied to the memory device are, in each case,

compared simultaneously by all comparison units with the portion of the reference addresses associated with each active comparison unit, that is to say **simultaneously with all portions of the reference addresses.**

As explained on page 20, each comparison unit may be individually activated or deactivated. In this way the comparison units described in the instant application may be used, based on how much of the address is provided, more like a bit level check or block level check than those more general tests shown in **NOSE**.

The **NOSE** reference discloses a semiconductor memory for a display capable of relieving a defective memory cell by exchanging addresses. More specifically, the converting circuit outputs the address stored in a second memory circuit when an address supplied from an external address input coincides with the address stored in a first memory circuit. As mission critical semiconductor memory, display memory should be checked regularly to ensure a proper display. Accordingly, a self-test circuit 14 in **NOSE** operates at power-on time and the like to test the memory operations of all memory addresses (col. 5, lines 12-15). The self-test circuit provides the address, the writing data, and the expected value to check the memory operations of the main

memory 16. Any address found to be faulty is stored in memory circuit 13. After the self-test, the memory checks the address of a requested memory and if it matches then the spare memory 17 is activated and the data is stored or retrieved from the spare memory 17, depending on the nature of the original request.

As correctly indicated on page 3 of the above-identified final Office Action, **NOSE** does not explicitly teach "the simultaneous checking by comparator means." However, as will be explained below, the Examiner incorrectly asserts that **BOSSE** makes up for this deficiency.

Clearly, **NOSE** does not show comparison units "to simultaneously check" whether a received address is associated with at least one memory cell or memory cell areas that cannot be properly written as recited in claim 1 of the instant application.

The newly cited **BOSSE** reference discloses a method and an apparatus for rapidly testing arrays of cells, such as memory devices, in which a limited number of redundancy rows and columns are available for repair. Repairs in **BOSSE** are made by the substitution of redundant rows and columns for original rows and columns of the array that contain the

faulty cells. The repair information as to whether a row or a column is to be substituted for a faulty original cell is determined in **BOSSE**, at least in part, in real time **as the cells are being sequentially tested**. (*see e.g.*, Abstract and col.6 lines 63-66). **BOSSE** teaches **"sequential testing"** NOT "to simultaneously check" as recited in claim 1 of the instant application.

Clearly, **BOSSE** does not show comparison units **"to simultaneously check"** whether a received address is associated with at least one memory cell or memory cell areas that cannot be properly written as recited in claim 1 of the instant application.

As indicated in MPEP § 2142 "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Moreover, to establish a *prima facie* case of obviousness, MPEP § 2142 explains that three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the

reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). In the instant case, it is clear that **BOSSE expressly teaches away from the Examiner's proposed combination** by indicating that the individual cells of the device under test are "sequentially tested" and not simultaneously checked as required by the claims of the instant application. As such, applicant respectfully submits that a *prima facie* case has NOT been produced.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-27 are solicited.

In the event the Examiner should still find any of the remaining claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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